Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

1.(original) A defect analysis apparatus for a semiconductor integrated circuit characterized in that a presence/absence of a defect is detected by irradiating an electromagnetic field from a probe and detecting a power supply current variation.

2.(original) A defect analysis apparatus for a semiconductor integrated circuit characterized in that a presence/absence of a defect is detected by irradiating an electromagnetic field from a probe and detecting a voltage variation, an impedance variation or an electric characteristic variation.

3.(currently amended)The defect analysis apparatus for a semiconductor integrated circuit according to claim 1 ~~or 2~~, characterized in that said power supply current variation, said voltage variation, or said impedance variation is detected by activating an open gate or a gate potential.

4.(currently amended)The defect analysis apparatus for a semiconductor integrated circuit according to ~~any one of~~ claims 1 ~~to 3~~, characterized in that said power supply current variation, said voltage variation or said impedance variation is detected by exciting the probe with modulation and synchronizing with a signal applied to the probe.

5. (currently amended)The defect analysis apparatus for a semiconductor integrated

circuit according to ~~any one of~~ claims 1 ~~to 4~~, characterized in that a defect is detected by measuring heat radiation and light emission radiation caused by said power supply current variation, said voltage variation or said impedance variation.

6.(original) A defect analysis apparatus for a semiconductor integrated circuit characterized in that an electric characteristic variation in the semiconductor integrated circuit is detected by activating an open gate or a gate potential.

7.(currently amended)The defect analysis apparatus for a semiconductor integrated circuit according to claim ~~5~~6, characterized in that a power supply current variation is applied to the semiconductor integrated circuit and the open gate or the gate potential is activated.

8.(currently amended)The defect analysis apparatus for a semiconductor integrated circuit according to claim 6 ~~or 7~~, characterized in that the open gate or the gate potential is activated by irradiating an electromagnetic field from a probe.

9.(original)The defect analysis apparatus for a semiconductor integrated circuit according to claim 8, characterized in that said electric characteristic variation is detected by exciting the probe with modulation and synchronizing with a signal applied to the probe.

10.(currently amended)The defect analysis apparatus for a semiconductor integrated circuit according to ~~any one of~~ claims 1 ~~to 9~~, characterized in that a defect position is identified from differential information on a defective product and on a normal product.

11.(currently amended)The defect analysis apparatus for a semiconductor integrated circuit according to ~~any one of~~ claims ~~1~~3 ~~to 10~~, characterized in that irradiation of an

electromagnetic field from the probe or activation of the open gate or the gate potential is performed on a substrate side.

12.(currently amended)The defect analysis apparatus for a semiconductor integrated circuit according to ~~any one of~~ claim~~s~~ 1 ~~to 11~~, characterized in that a defect portion is determined by mutually referring to position information on the probe and design information on a chip.

13.(original) The defect analysis apparatus for a semiconductor integrated circuit according to claim 12, characterized in that if a defect portion and a detected abnormal portion are different, a wiring path of a wiring including an area of the detected abnormal portion is analyzed by referring to design data.

14.(original) A manufacture method for a semiconductor device comprising: a design step of designing a wiring pattern of the semiconductor device; a manufacture step of manufacturing the semiconductor device in accordance with the design information; an inspection step of inspecting the manufactured semiconductor device or the semiconductor device during manufacture; and an analysis/evaluation step of analyzing or evaluating the test result, wherein the analysis/evaluation step irradiates an electromagnetic field from a probe to a wiring of the semiconductor device, and detects a defect portion by detecting a power supply current variation, the semiconductor device is manufactured if the defect result clears predetermined conditions, whereas a defect reason is identified in accordance with the analysis result if the defect result does not clear the predetermined conditions, and the defect reason is fed back to manufacture processes.

15.(new) The defect analysis apparatus for a semiconductor integrated circuit according to claim 2, characterized in that said voltage variation or said impedance variation is detected by activating an open gate or a gate potential.

16.(new) The defect analysis apparatus for a semiconductor integrated circuit according to claim 2, characterized in that said voltage variation or said impedance variation is detected by exciting the probe with modulation and synchronizing with a signal applied to the probe.

17.(new) The defect analysis apparatus for a semiconductor integrated circuit according to claim 2, characterized in that a defect is detected by measuring heat radiation and light emission radiation caused by said voltage variation or said impedance variation.